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## Electrical Specification

## Internal Logic Power Recommended operating conditions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameters** | **Symbol** | **Min** | **Typ** | **Max** | **Units** |
| Internal digital logic power | VDD | 0.8 | 0.9 | 1 | V |
| Supply voltage for CUP | CA7\_VDD | 0.8 | 0.9 | 1.1 | V |
| Supply voltage for DSP | CEVA\_VDD | 0.8 | 0.9 | 1.1 | V |
| Supply voltage for OTP | OTP\_VDDIO1V8 | 1.62 | 1.8 | 1.98 | V |

## Digital IO Electrical Characteristics

## DC Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Parameters** | | **Symbol** | **Min** | **Typ** | **Max** | **Units** |
| Digital general IO @1.8V | Input Low Voltage | VIL | -0.3 |  | 0.63 | V |
| Input High Voltage | VIH | 1.17 |  | 1.98 | V |
| Threshold Point | VT | 0.83 | 0.91 | 1 | V |
| Schmitt Trigger Low to High Threshold Point | VT+ | 0.95 | 1.03 | 1.11 | V |
| VT- | 0.67 | 0.79 | 0.9 | V |
| Input Leakage Current @VI=1.8V or 0V | II |  |  | ±10μ | A |
| Tri-state Output Leakage Current @VO=1.8V or 0V | IOZ |  |  | ±10μ | A |
| Pull-up Resistor | RPU | 54k | 80k | 120k | Ω |
| Pull-down Resistor | RPD | 55k | 95k | 176k | Ω |
| Output Low Voltage | VOL |  |  | 0.45 | V |
| Output High Volgate | VOH | 1.35 |  |  | V |
| Low Level Output Current @VOL(max) | IOL | | | | |
| 00 | 7.4 | 12.2 | 17.4 | mA |
| 01 | 14.8 | 24.3 | 34.5 | mA |
| 10 | 22.1 | 36.2 | 51.0 | mA |
| 11 | 29.3 | 47.8 | 66.6 | mA |
| Low Level Output Current @VOH(min) | IOH | | | | |
| 00 | 4.9 | 11.0 | 19.8 | mA |
| 01 | 9.8 | 21.9 | 39.5 | mA |
| 10 | 14.6 | 32.9 | 59.1 | mA |
| 11 | 19.5 | 43.7 | 78.6 | mA |
| Digital SD IO | Input Low Voltage | VIL | -0.3 |  | 0.7125 | V |
| Input High Voltage | VIH | 1.875 |  | 3.15 | V |
| Threshold Point | VT | 0.81 | 0.95 | 1.12 | V |
| Schmitt Trigger Low to High Threshold Point | VT+ | 1 | 1.1 | 1.23 | V |
| VT- | 0.74 | 0.9 | 1.08 | V |
| Input Leakage Current @VI=1.8V or 0V | II |  |  | ±10μ | A |
| Tri-state Output Leakage Current @VO=1.8V or 0V | IOZ |  |  | ±10μ | A |
| Pull-up Resistor | RPU | 33k | 59k | 89k | Ω |
| Pull-down Resistor | RPD | 34k | 61k | 95k | Ω |
| Output Low Voltage | VOL |  |  | 0.35625 | V |
| Output High Volgate | VOH | 2.1375 |  |  | V |
| Low Level Output Current @VOL(max) | IOL | | | | |
| 000 | 3.2 | 5.4 | 8.3 | mA |
| 001 | 4.7 | 8.0 | 12.3 | mA |
| 010 | 6.3 | 10.7 | 16.4 | mA |
| 011 | 7.8 | 13.2 | 20.2 | mA |
| 100 | 9.4 | 15.9 | 24.2 | mA |
| 101 | 10.9 | 18.4 | 28.1 | mA |
| 110 | 12.4 | 20.9 | 31.8 | mA |
| 111 | 13.9 | 23.4 | 35.5 | mA |
| Low Level Output Current @VOH(min) | IOH | | | | |
| 000 | 5.0 | 7.6 | 11.2 | mA |
| 001 | 7.5 | 11.4 | 16.8 | mA |
| 010 | 10.0 | 15.2 | 22.3 | mA |
| 011 | 12.4 | 18.9 | 27.8 | mA |
| 100 | 14.9 | 22.6 | 33.3 | mA |
| 101 | 17.4 | 26.3 | 38.7 | mA |
| 110 | 19.8 | 30.0 | 44.1 | mA |
| 111 | 22.3 | 33.7 | 49.5 | mA |
| Digital RGMII IO | Input Low Voltage | VIL | -0.3 |  | 0.8 | V |
| Input High Voltage | VIH | 2.0 |  | 3.465 | V |
| Threshold Point | VT | 1.02 | 1.18 | 1.37 | V |
| Schmitt Trigger Low to High Threshold Point | VT+ | 1.23 | 1.34 | 1.5 | V |
| VT- | 0.97 | 1.13 | 1.33 | V |
| Input Leakage Current @VI=1.8V or 0V | II |  |  | ±10μ | A |
| Tri-state Output Leakage Current @VO=1.8V or 0V | IOZ |  |  | ±10μ | A |
| Pull-up Resistor | RPU | 26k | 46k | 71k | Ω |
| Pull-down Resistor | RPD | 27k | 48k | 102k | Ω |
| Output Low Voltage | VOL |  |  | 0.4 | V |
| Output High Volgate | VOH | 2.4 |  |  | V |
| Low Level Output Current @VOL(max) | IOL | | | | |
| 000 | 4.0 | 6.3 | 8.9 | mA |
| 001 | 6.0 | 9.4 | 13.3 | mA |
| 010 | 8.0 | 12.6 | 17.7 | mA |
| 011 | 10.0 | 15.6 | 21.9 | mA |
| 100 | 12.0 | 18.7 | 26.2 | mA |
| 101 | 14.0 | 21.8 | 30.4 | mA |
| 110 | 15.9 | 24.7 | 34.5 | mA |
| 111 | 17.8 | 2707 | 38.5 | mA |
| Low Level Output Current @VOH(min) | IOH | | | | |
| 000 | 6.0 | 9.3 | 14.2 | mA |
| 001 | 9.0 | 14.0 | 21.3 | mA |
| 010 | 12.1 | 18.6 | 28.4 | mA |
| 011 | 15.1 | 23.3 | 35.5 | mA |
| 100 | 18.1 | 27.9 | 42.6 | mA |
| 101 | 21.1 | 32.5 | 49.7 | mA |
| 110 | 24.1 | 37.2 | 56.8 | mA |
| 111 | 27.1 | 41.8 | 63.8 | mA |

## PCIE electrical Characteristics

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **2.5 GT/s** | **5.0 GT/s** | **Unit** | **Comments** |
| **Transmitter Specifications** | | | | | |
| UI | Unit Interval | 399.88  (min)  400.12  (max) | 199.94  (min)  200.06  (max) | ps | The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations. See Note 1. |
| VTX-DIFF-PP | Differential p-p Tx voltage swing | 0.8 (min)  1.2 (max) | 0.8 (min)  1.2 (max) | V | As measured with compliance test load. Defined as 2\*|VTXD+ - VTXD- |. |
| VTX-DIFF-PP-LOW | Low power differential p-p Tx voltage swing | 0.4 (min)  1.2 (max) | 0.4 (min)  1.2 (max) | V | As measured with compliance test load. Defined as 2\*|VTXD+ - VTXD- |. See Note 9. |
| VTX-DE-RATIO-3.5dB | Tx de-emphasis level ratio | 3.0 (min)  4.0 (max) | 3.0 (min)  4.0 (max) | dB | See Note 11 for details. |
| VTX-DE-RATIO-6dB | Tx de-emphasis level | N/A | 5.5 (min)  6.5 (max) | dB | See Note 11 for details |
| TMIN-PULSE | Instantaneous lone pulse width | Not specified | 0.9 (min) | UI | Measured relative to rising/falling pulse. See Notes 2, 10. |
| TTX-EYE | Transmitter Eye including all jitter sources | 0.75 (min) | 0.75 (min) | UI | Does not include SSC or Refclk jitter. Includes Rj at 10-12. See Notes 2, 3, 4, and 10. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods. |
| TTX-EYE-MEDIAN-to-MAX-JITTER | Maximum time between the jitter median and max deviation from the median | 0.125 (max) | Not specified | UI | Measured differentially at zero crossing points after applying the 2.5 GT/s clock recovery function. See Note 2. |
| TTX-HF-DJ-DD | Tx deterministic jitter > 1.5 MHz | Not specified | 0.15 (max) | UI | Deterministic jitter only. See Notes 2 and 10. |
| TTX-LF-RMS | Tx RMS jitter < 1.5 MHz | Not specified | 3.0 | ps  RMS | Total energy measured over a 10 kHz –1.5 MHz range. |
| TTX-RISE-FALL | Transmitter rise and fall time | 0.125 (min) | 0.15 (min) | UI | Measured differentially from 20% to 80% of swing. See Note 2. |
| TRF-MISMATCH | Tx rise/fall mismatch | Not specified | 0.1 (max) | UI | Measured from 20% to 80% differentially. See Note 2. |
| BWTX-PLL | Maximum Tx PLL bandwidth | 22 (max) | 16 (max) | MHz | Second order PLL jitter transfer bounding function. See Note 6 |
| BWTX-PLL-LO-3DB | Minimum Tx PLL BW for 3 dB  peaking | 1.5 (min) | 8 (min) | MHz | Second order PLL jitter transfer bounding function. See Notes 6 and 8. |
| BWTX-PLL-LO-1DB | Minimum Tx PLL BW for 1 dB  peaking | Not specified | 5 (min) | MHz | Second order PLL jitter transfer bounding function. See Notes 6 and 8. |
| PKGTX-PLL1 | Tx PLL peaking with 8 MHz min  BW | Not specified | 3.0 (max) | dB | Second order PLL jitter transfer bounding function. See Notes 6 and 8. |
| PKGTX-PLL2 | Tx PLL peaking with 5 MHz min BW | Not specified | 1.0 (max) | dB | See Note 8. |
| RLTX-DIFF | Tx package plus Si differential return loss | 10 (min) | 10 (min) for 0.05 -1.25 GHz  8 (min) for1.25 -2.5 GHz | dB |  |
| RLTX-CM | Tx package plus Si common mode return loss | 6 (min) | 6 (min) | dB | Measured over 0.05 – 1.25 GHz range for 2.5 GT/s and 0.05 – 2.5 GHz range for 5.0 GT/s. (S11 parameter) |
| ZTX-DIFF-DC | DC differential Tx impedance | 80 (min)  120 (max) | 120 (max) | Ω | Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF. |
| VTX-CM-AC-PP | Tx AC common mode voltage (5.0 GT/s) | Not specified | 100 (max) | mVPP | See Note 5. |
| VTX-CM-AC-P | Tx AC common mode voltage (2.5 GT/s) | 20 | Not specified | mV | See Note 5. |
| ITX-SHORT | Transmitter short-circuit current limit | 90 (max) | 90 (max) | mA | The total current Transmitter can supply when shorted to ground. |
| VTX-DC-CM | Transmitter DC common-mode voltage | 0 (min)  3.6 (max) | 0 (min)  3.6 (max) | V | The allowed DC common-mode voltage at the Transmitter pins under any conditions |
| VTX-CM-DC-ACTIVEIDLE-DELTA | Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle. | 0 (min)  100 (max) | 0 (min)  100 (max) | mV | |VTX-CM-DC [during L0] – VTX-CM-Idle-DC [during Electrical Idle]|<= 100 mV  VTX-CM-DC = DC(avg) of |VTX-D+ + VTX-D-|/2  VTX-CM-Idle-DC= DC(avg) of |VTX-D+ + VTX-D-|/2  [Electrical Idle] |
| VTX-CM-DC-LINEDELTA | Absolute Delta of DC Common Mode Voltage between D+ and D- | 0 (min)  25 (max) | 0 (min)  25 (max) | mV | |VTX-CM-DC-D+ [during L0] – VTX-CM-DC-D- [during L0.]| ≤ 25mV  VTX-CM-DC-D+ = DC(avg) of |VTX-D+| [during L0]  VTX-CM-DC-D- = DC(avg) of |VTX-D-| [during L0] |
| VTX-IDLE-DIFF-AC-p | Electrical Idle Differential Peak Output Voltage | 0 (min)  20 (max) | 0 (min)  20 (max) | mV | VTX-IDLE-DIFFp = |VTX-Idle-D+ - VTx-Idle-D-| ≤ 20 mV.  Voltage must be high pass filtered to remove any DC component. |
| VTX-IDLE-DIFF-DC | DC Electrical Idle Differential Output Voltage | Not specified | 0 (min)  5 (max) | mV | VTX-IDLE-DIFF-DC = |VTX-Idle-D+ - VTx-Idle-D-| ≤ 5 mV.  Voltage must be low pass filtered to remove any AC component. Filter characteristics complementary to above. |
| VTX-RCV-DETECT | The amount of voltage change allowed during Receiver Detection | 600 (max) | 600 (max) | mV | The total amount of voltage change in a positive direction that a Transmitter can apply to sense whether a low impedance Receiver is present. Note: Receivers display substantially different impedance for VIN <0 vs VIN > 0. |
| TTX-IDLE-MIN | Minimum time spent in Electrical Idle | 20 (min) | 20 (min) | ns | Minimum time a Transmitter must be in Electrical Idle. |
| TTX-IDLE-SET-TOIDLE | Maximum time to transition to a valid Electrical Idle after sending an EIOS | 8 (max) | 8 (max) | ns | After sending the required number of EIOSs, the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EIOS to the Transmitter in Electrical Idle. |
| TTX-IDLE-TO-DIFFDATA | Maximum time to transition to valid diff signaling after leaving Electrical Idle | 8 (max) | 8 (max) | ns | Maximum time to transition to valid diff signaling after leaving Electrical Idle. This is considered a debounce time to the Tx. |
| TCROSSLINK | Crosslink random timeout | 1.0 (max) | 1.0 (max) | ms | This random timeout helps resolve potential conflicts in the crosslink configuration. |
| LTX-SKEW | Lane-to-Lane Output Skew | 500 ps + 2 UI (max) | 500 ps + 4 UI (max) | ps | Between any two Lanes within a single Transmitter. |
| CTX | AC Coupling Capacitor | 75 (min)  200 (max) | 75 (min)  200 (max) | nF | All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. |
| **Notes** | 1. SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.  2. Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device’s pins, although deconvolution is recommended. At least 106 UI of data must be acquired.  3. Transmitter jitter is measured by driving the Transmitter under test with a low jitter “ideal” clock and connecting the DUT to a reference load.  4. Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5 GT/s and 5.0 GT/s use different filter functions. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.  5. Measurement is made over at least 106 UI.  6. The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table.  7. Measurements are made for both common mode and differential return loss. The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value  8. A single combination of PLL BW and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two combinations of PLL BW and peaking are specified to permit designers to make a tradeoff between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the max PLL BW is 16 MHz.  9. Low swing output, defined by VTX-DIFF-PP-LOW must be implemented with no de-emphasis.  10. For 5.0 GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied. This parameter is measured by accumulating a record length of 106 UI while the DUT outputs a compliance pattern. TMIN-PULSE is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity.  11. Root complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5 GT/s. | | | | |
| **Receiver Specifications** | | | | | |
| UI | Unit Interval | 399.88  (min)  400.12  (max) | 199.94  (min)  200.06  (max) | ps | UI does not account for SSC caused variations. |
| VRX-DIFF-PP-CC | Differential Rx peak-peak voltage for common Refclk Rx architecture | 0.175 (min)  1.2 (max) | 0.120 (min)  1.2 (max) | V |  |
| VRX-DIFF-PP-DC | Differential Rx peak-peak voltage for data clocked Rx architecture | 0.175 (min)  1.2 (max) | 0.100 (min)  1.2 (max) | V |  |
| TRX-EYE | Receiver eye time opening | 0.40 (min) | N/A | UI | Minimum eye time at Rx pins to yield a 10-12 BER. See Note 1. |
| TRX-TJ-CC | Max Rx inherent timing error | N/A | 0.40 (max) | UI | Max Rx inherent total timing error for common Refclk Rx architecture. See Note 2. |
| TRX-TJ-DC | Max Rx inherent timing error | N/A | 0.34 (max) | UI | Max Rx inherent total timing error for data clocked Rx architecture. See Note 2. |
| TRX-DJ-DD-CC | Max Rx inherent deterministic timing error | N/A | 0.30 (max) | UI | Max Rx inherent deterministic timing error for common Refclk Rx architecture. See Note 2. |
| TRX-DJ-DD-DC | Max Rx inherent deterministic timing error | N/A | 0.24 (max) | UI | Max Rx inherent deterministic timing error for data clocked Rx architecture. See Note 2. |
| TRX-EYE-MEDIAN-to-MAX-JITTER | Max time delta between median and deviation from median | 0.3 (max) | Not specified | UI | Only specified for 2.5 GT/s. |
| TRX-MIN-PULSE | Minimum width pulse at Rx | Not specified | 0.6 (min) | UI | Measured to account for worst Tj at 10-12 BER. |
| VRX-MAX-MIN-RATIO | min/max pulse voltage on consecutive UI | Not specified | 5 (max) | -- | Rx eye must simultaneously meet VRX\_EYE limits. |
| BWRX-PLL-HI | Maximum Rx PLL bandwidth | 22 (max) | 16 (max) | MHz | Second order PLL jitter transfer bounding function . See Note 3. |
| BWRX-PLL-LO-3DB | Minimum Rx PLL BW for 3 dB peaking | 1.5 (min) | 8 (min) | MHz | Second order PLL jitter transfer bounding function. See Note 3. |
| BWRX-PLL-LO-1DB | Minimum Rx PLL BW for 1 dB peaking | Not specified | 5 (min) | MHz | Second order PLL jitter transfer bounding function. See Note 3. |
| PKGRX-PLL1 | Rx PLL peaking with 8 MHz min BW | Not specified | 3.0 | dB | Second order PLL jitter transfer bounding function . See Note 3. |
| PKGRX-PLL2 | Rx PLL peaking with 5 MHz min BW | Not specified | 1.0 | dB | Second order PLL jitter transfer bounding function. See Note 3. |
| RLRX-DIFF | Rx package plus Si differential return loss | 10 (min) | 10 (min) for 0.05 - 1.25 GHz  8 (min) for 1.25 - 2.5 GHz | dB | See Note 4. |
| RLRX-CM | Common mode Rx return loss | 6 (min) | 6 (min) | dB | See Note 4. |
| ZRX-DC | Receiver DC common mode impedance | 40 (min)  60 (max) | 40 (min)  60 (max) | Ω | DC impedance limits are needed to guarantee Receiver detect. See Note 5. |
| ZRX-DIFF-DC | DC differential impedance | 80 (min)  120 (max) | Not specified | Ω | For 5.0 GT/s covered under RLRX-DIFF parameter. See Note 5. |
| VRX-CM-AC-P | Rx AC common mode voltage | 150 (max) | 150 (max) | mVP | Measured at Rx pins into a pair of 50 Ω terminations into ground. See Note 6. |
| ZRX-HIGH-IMP-DCPOS | DC Input CM Input Impedance for V>0 during Reset or power down | 50 k (min) | 50 k (min) | Ω | Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 200 mV with respect to ground. See Note 7. |
| ZRX-HIGH-IMP-DCNEG | DC Input CM Input Impedance for V<0 during Reset or power down | 1.0 k (min) | 1.0 k (min) | Ω | Rx DC CM impedance with the Rx terminations not powered, measured over the range -150 – 0 mV with respect to ground. See Note 7. |
| VRX-IDLE-DETDIFFp-p | Electrical Idle Detect Threshold | 65 (min)  175 (max) | 65 (min)  175 (max) | mV | VRX-IDLE-DET-DIFFp-p = 2\*|VRX-D+ - VRXD-|. Measured at the package pins of the Receiver. |
| TRX-IDLE-DET-DIFFENTERTIME | Unexpected Electrical Idle Enter Detect Threshold Integration Time | 10 (max) | 10 (max) | ms | An unexpected Electrical Idle (VRXDIFFp-p < VRX-IDLE-DET-DIFFp-p) must be recognized no longer than TRX-IDLEDET-DIFF-ENTERTIME to signal an unexpected idle condition. |
| LRX-SKEW | Lane to Lane skew | 20 (max) | 8 (max) | ns | Across all Lanes on a Port. This includes variation in the length of a SKP Ordered Set at the Rx as well as any delay differences arising from the interconnect itself. See Note 8. |
| **Notes** | 1. Receiver eye margins are defined into a 2 x 50 Ω reference load.  2. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.  3. Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make tradeoffs between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined.  4. Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.  5. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.  6. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V-CMDC|}.  7. ZRX-HIGH-IMP-DC-NEG and ZRX-HIGH-IMP-DC-POS are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.  8. The LRX-SKEW parameter exists to handle repeaters that regenerate Refclk and introduce differing numbers of skips on different Lanes. | | | | |

## TYPEC electrical Characteristics

## Operating Conditions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Name | Min | Typ | Max | Units | Description |
| Vavdd\_cmn\_clk | 0.813 | 0.9 | 1.0 | V | Core supply voltage at the junction. Refer to Table ‘Power supply budget’. |
| Vavdd\_h | 1.58 | 1.8 | 1.994 | V | IO supply voltage at the junction. Refer to Table ‘Power supply budget’ |
| Vavdd\_tx\_<> | 0.813 | 0.9 | 1.0 | V | Core supply voltage at the junction. Refer to Table ‘Power supply budget’. |
| Vavdd\_xcvr | 0.813 | 0.9 | 1.0 | V | Core supply voltage at the junction. Refer to Table ‘Power supply budget’. |
| Vavdd\_xcvr\_clk\_<> | 0.813 | 0.9 | 1.0 | V | Core supply voltage at the junction. Refer to Table ‘Power supply budget’. |
| Tj | -40 | 25 | 125 | ℃ | Junction temperature |

## Power supply budgeting

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Name | Voltage | | | | | Description |
| Min | Typ | | | Max |
| Supply Budgeting for avdd and avdd\_clk: 0.9V | | | | | | |
| Off die VRM DC variation | -3.50% | |  | 8.50% | | On board voltage regulator DC accuracy. |
| Off die VRM AC VRM noise | 2.00% | | | | | Peak-to-peak 18mV frequency content: 50KHz to 500KHz |
| 1.00% | | | | | Peak-to-peak 9mV with frequency content: 500KHz to 10MHz; no single frequency noise amplitude can be more than 5mV. |
| Off die total supply variation | -5.0% | | - | 10.0% | | Total off-die voltage variation at package pin of supply die to external voltage regulator. |
| AC Self Induced + Coupling Noise | 1.70% | | | | | This 15.3mV peak-to-peak noise due to switching current through package parasitics. This is wideband. |
| Package IR (DC) drop | -1.0% | | - | 0.00% | | The 9mV IR drop is due to worst case DC current of the PHY. |
| On die IR (DC) drop | -2.50% | | - | 0.00% | | The 22.5mV drop is due to worst case DC current and worst case metal routing parasitic. |
| Final Voltage range (V) | 0.813 | | 0.90 | 1.00 | | This is the expected voltage at the junction. It includes 2.7mV margin for the design. |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Name | Voltage | | | | | Description |
| Min | Typ | | | Max |
| Supply Budgeting for 1.8V IO supply (avdd\_h) | | | | | | |
| Off die VRM DC variation | -8.50% | |  | 8.50% | | On board voltage regulator DC accuracy. |
| Off die VRM AC VRM noise | 2.00% | | | | | Peak-to-peak 36mV frequency content: 50KHz to 500KHz |
| 1.00% | | | | | Peak-to-peak 18mV with frequency content: 500KHz to 10MHz. |
| Off die total supply variation | -10.0% | | - | 10.0% | | Total off-die voltage variation at package pin of supply due to external voltage regulator. |
| AC Self Induced + Coupling Noise | 0.50% | | | | | This 9mV peak-to-peak noise is due to switching current through package parasitics. This is wideband. |
| Package IR (DC) drop | -0.5% | | - | 0.00% | | This 9mV IR drop is due to worst case DC current of the PHY |
| On die IR (DC) drop | -1.00% | | - | 0.00% | | This 18mV drop is due to worst case DC current and worst case metal routing parasitic. |
| Final Voltage range (V) | -1.58 | | 1.8 | 1.994 | | This is the expected voltage at the junction. It includes 0.5mV margin for the design. |

## Common Electrical Specifications

## Reference Clock Input Specifications

Minimize exposure to nearby aggressor signals that could contaminate the clock with crosstalk, especially if these signals are lower than 1MHz in frequency.

If these bumps are not used, it is not necessary to AC couple or terminate these pins. They can be left floating.

Reference clock specification for USB3 and DP

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Normative Electrical Parameters | Min | Typ | Max | Units | Description |
| External Clock Frequency | - | 24 | - | MHz | - |
| Input Duty Cycle | 48 | - | 52 | % | - |
| Single-ended clock input voltage (CMOS level) | 0.85 | - | 1 | V | - |
| Input Random Jitter | - | - | 140 | dBC/Hz | Noise floor density from 10 KHz to 10 MHz |
| - | - | 2.9 | ps | For a 24MHz  reference,integrated jitter from 10KHz to 10MHz |
| Input determinestic Jitter | - | - | 4 | ps | Over a band of 10KHz to 10MHz |

## DP Transmitter electrical specification

DP Transmitter module electrical Specifications

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Symbol | Description | Min | Typ | Max | Units | Comments |
| UI | UI\_HBR2 | 185.129 | 185 | 186.172 | ps | -Unit Interval for high bit  rate (DP: 5.4Gbps/  lane). Frequency ppm  -5300 to +300 |
| USB3 | 199.94 | 200 | 200.06 | UI with ± 300ppm with-  out SSC |
| UI\_HBR | 370.259 | 370 | 372.343 | Unit Interval for high bit  rate (DP: 2.7Gbps/  lane). Frequency ppm  -5300 to +300 |
| UI\_RBR | 617.098 | 617 | 620.573 | Unit Interval for high bit  rate (DP: 1.62Gbps/  lane). Frequency ppm  -5300 to +300 |
| VTX-DIFFp-p | Differential p-p TX voltage swing  including low power | 100 | - | 1200 | mV | For USB 3.0, no EQ is  required. |
| ITX-SHORT | Transmit lane short-circuit current | - | - | 100 | mA | - |
| RLTX-DIFF | Transmitter differential return loss | - | - | 0 < -20dB < 100Mhz  100Mhz < -18dB < 300Mhz  300Mhz < -16dB < 600Mhz  600Mhz < -10dB < 2500Mhz  2500Mhz < -9dB < 4875Mhz  4875Mhz < -8dB < 11200Mhz  11200Mhz < -5dB <  16800Mhz  and -3dB beyond that | db |  |
| RLTX-CM | Transmitter common mode return  loss | - | - | 50Hz < -8dB < 15000Mhz | dB |  |
| ZTX\_cal | DC differential TX impedance. Cali-  brated differential driver imped-  ance when in normal mode. | 80 | 100 | 120 | Ω |  |
| T20-80TX | TX Rise/Fall Time | - | - | 0.41 | UI |  |
| TskewTX | TX Differential Skew | 20 | - | 30 | ps |  |
| JTT | Transmitter total jitter (peak-to-  peak) (Tj) | - | - | 65 |  | USB3.0 |
| - | - |  |  | Edp/dp |
| TTX-RJ-PLL | Random jitter (Max) | - | - | 1.4 | Ps rms | USB3.0 and DP is after TXLF |
| TTX-IDLE-TO-DIFF-  DATA | Maximum time to transition to valid  diff signaling after leaving Electrical  Idle | - | - | 8 | ns |  |
| TEIExit | Time to exit Electrical Idle (L0s)  state and to enter L0 | - | - | 5 | Txsys-clk |  |

## USB electrical Characteristics

|  |  |  |
| --- | --- | --- |
| **Power Supply** | **Ball Name** | **Value** |
| High-voltage power supply | USB\_VDD3V3 | 3.3 V (+ 10%, - 7%) at the macro pins with respect to gd (ground) |
| High-voltage power supply | USB\_VDDH3V3 | 3.3 V (+ 10%, - 7%) at the macro pins with respect to gd (ground) |
| Low-voltage supply | USB\_DVDD0V9 | 0.90 V (+ 10%, - 7%) at the macro pins with respect to gd (ground) |
| Low-voltage supply | USB\_VP0V9 | 0.90 V (+ 10%, - 7%) at the macro pins with respect to gd (ground) |

## USB 3.0 Transmitter Normative Electrical Parameters

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **5.0 GT/s** | **Units** | **Comments** |
| UI | Unit Interval | 199.94 (min)  200.06 (max) | ps | The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations |
| VTX-DIFF-PP | Differential p-p Tx voltage swing | 0.8 (min)  1.2 (max) | V | Nominal is 1 V p-p |
| VTX-DE-RATIO | Tx de-emphasis | 3.0 (min)  4.0 (max) | dB | Nominal is 3.5 dB |
| RTX-DIFF-DC | DC differential impedance | 72 (min)  120 (max) | Ω |  |
| VTX-RCV-DETECT | The amount of voltage change allowed during Receiver Detection | 0.6 (max) | V | Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an “off” receiver’s input goes below ground. See Section 1.2.5.6 and Note 9 for details |
| CAC-COUPLING | AC Coupling Capacitor | 75 (min) 200 (max) | nF | All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. |
| TCDR\_SLEW\_MAX | Max slew rate | 10 | ms/sec | See the jitter white paper for details on this measurement. |
| TMIN-PULSE-Dj | Deterministic min pulse | 0.96 | UI | Tx pulse width variation that is deterministic. |
| TMIN-PULSE-Tj | Tx min pulse | 0.90 | UI | Min Tx pulse at 10-12 including Dj and Rj. |
| TTX-EYE | Transmitter Eye | 0.625 (min) | UI | Includes all jitter sources |
| TTX—DJ-DD | Tx deterministic jitter | 0.19 (max) | UI | Deterministic jitter only assuming the Dual Dirac distribution |
| CTX-PARASITIC | Tx input capacitance for return loss | 1.25 (max) | pf | Parasitic capacitance to ground |
| RTX-DC | Transmitter DC common mode impedance | 18 (min)  30 (max) | Ω | DC impedance limits to guarantee Receiver detect behavior. Measured with respect to AC ground over a voltage of 0-500mV. |
| ITX-SHORT | Transmitter shortcircuit current limit | 60 (max) | mA | The total current Transmitter can supply when shorted to ground. |
| VTX-DC-CM | Transmitter DC common-mode voltage | 0 (min) 2.2 (max) | V | The instantaneous allowed DC common-mode voltages at the connector side of the AC coupling capacitors. |
| VTX-CM-ACPP\_ACTIVE | Tx AC common mode voltage active | 100 mv | mVPP | Max mismatch from D+ D- for both time and amplitude. While signaling. |
| VTX-CM-DC-ACTIVEIDLE-DELTA | Absolute Common Mode Voltage between *U1* and *U0* | 200 (max) | mV | peak |
| VTX-IDLE-DIFF-AC-pp | Electrical Idle Differential Peak – Peak Output Voltage | 0 (min)  10 (max) | mV |  |
| VTX-IDLE-DIFF-DC | DC Electrical Idle Differential Output Voltage | 0 (min)  10 (max) | mV | Voltage must be low pass filtered to remove any AC component. This limits the common mode error when resuming U1 to U0 |

## USB 3.0 Receiver Electrical Parameters

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **5.0 GT/s** | **Units** | **Comments** |
| UI | Unit Interval | 199.94 (min)  200.06 (max) | ps | UI does not account for SSC caused variations. |
| VRX-DIFF-PP-POST-EQ | Differential Rx peakpeak voltage | *30* (min) | mV | Measured after the Rx EQ function |
| TRX-TJ | Max Rx inherent timing error | *0.45* (max) | UI | Measured after the Rx EQ  function |
| TRX-DJ-DD | Max Rx inherent deterministic timing error | *0.3* (max) | UI | Max Rx inherent deterministic timing error |
| CRX-PARASITIC | Rx input capacitance for return loss | 1.1 (max) | pf |  |
| RRX-DC | Receiver DC common mode impedance | 18 (min)  30 (max) | Ω | DC impedance limits are needed to guarantee Receiver detect. Measured with respect to ground over a voltage of 500 mV max*.* |
| RRX-DIFF-DC | DC differential impedance | 72 (min)  120 (max) | Ω |  |
| VRX-CM-AC-P | Rx AC common mode voltage | 150 (max) | mV Peak | Measured at Rx pins into a pair of 50 Ω terminations into ground. Includes Tx and channel conversion, AC range up to 5 GHz |
| VRX-CM-DC-ACTIVEIDLE-DELTA\_P | Rx AC common mode voltage during the U1 to U0 transition | 200 (max) | mV Peak | Measured at Rx pins into a pair of 50 Ω terminations into ground. Includes Tx and channel conversion, AC range up to 5 GHz |
| ZRX-HIGH-IMP-DC-POS | DC Input CM Input Impedance for V>0 during Reset or power down | 25 k (min) | Ω | Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 500 mV with respect to ground. |
| VRX-LFPS-DET-DIFFp-p | LFPS Detect Threshold | 100 (min)  300 (max) | mV | Below the min is noise Must wake up above the max. |

## HDMI Electrical Characteristics

|  |  |
| --- | --- |
| **DC Characteristics** | |
| Item | value |
| Input Differential Voltage Level. | 150 |
| Input Common Mode Voltage, | If Sink supports only <=165M:  If sink supports >165Mhz |
|  |  |
| **When source Disabled or disconnected** | |
| Differential Voltage level |  |
| **AC input characteristics** | |
| Minimum differential sensitivity (peak-to-peak) | 150 mV |
| Maximum differential input (peak-to-peak) | 1560mV |
| Max Allowable Intra-Pair Skew at Sink Connector | For TMDS Clock rates 222.75MHz and below:  0.4 Tbit  For TMDS Clock rates above 222.75MHz:  0.15 Tbit + 112psecs |
| Max Allowable Inter-Pair Skew at Sink Connector | 0.2 Tcharacter + 1.78nsecs |
| TMDS Clock Jitter | 0.30 Tbit |
| **Impedance Characteristics** | |
| TDR Rise Time at TP2 (10%-90%) | ≤200 psec |
| Through connection impedance | 100 ohms ±15% |
| At Termination impedance  (when Vicm is within Vicm1 range) | 100 ohms ±10% |
| At Termination impedance  (when Vicm is within Vicm2 range) | 1. ms ±10% |

## MIPI Electrical Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Condition** | **Minimum** | **Typical** | **Maximum** | **Unit** |
| **Input DC Specifications** | | | | | | |
| VI | Input signal voltage range |  | -50 |  | 1350 | mv |
| ILEAK | Input leakage current | Note1 | -10 |  | 10 | μA |
| VGNDSH | Ground shift |  | -50 |  | 50 | mv |
| VOH(absmax) | Maximum transient output voltage level |  | -0.15 |  | 1.45 | v |
| tVOH(absmax) | Maximum transient time above VOH(absmax) |  |  |  | 20 | ns |
| **HS Line Drivers DC Specifications** | | | | | | |
| |VOD| | HS Transmit Differential output voltage magnitude | Note2 | 140 | 200 | 270 | mv |
| Δ|VOD| | Change in Differential output voltage magnitude between logic states | Note2 |  |  | 14 | mv |
| VCMTX | Steady-state  common-mode output  voltage | Note2 | 150 | 200 | 250 | mv |
| ΔVCMTX(1,0) | Changes in steady-state common-mode output voltage between logic states | Note2 |  |  | 5 | mv |
| VOHHS | HS output high voltage | Note2 |  |  | 360 | mv |
| ZOS | Single-ended output impedance |  | 40 | 50 | 62.5 | Ω |
| ΔZOS | Single-ended output  impedance mismatch |  |  |  | 10 | % |
| NOTE |  | | | | | |
| **LP Line Drivers DC Specifications** | | | | | | |
| VOL | Output low-level SE voltage |  | -50 |  | 50 | mv |
| VOH | Output high-level SE voltage |  | 1.1 | 1.2 | 1.3 | v |
| ZOLP | Single-ended output impedance |  | 110 |  |  | Ω |
| ΔZOLP(01,10) | Single-ended output impedance mismatch driving opposite level |  |  |  | 20 | % |
| ΔZOLP(00,11) | Single-ended output impedance mismatch driving same level |  |  |  | 5 | % |
| **HS Line Receiver DC Specifications** | | | | | | |
| VIDTH | Differential input high voltage threshold |  |  |  | 70 | mv |
| VIDTL | Differential input low voltage threshold |  | -70 |  |  | mv |
| VIHHS | Single ended input high voltage |  |  |  | 460 | mv |
| VILHS | Single ended input low voltage |  | -40 |  |  | mv |
| VCMRXDC | Input common mode voltage |  | 70 |  | 330 | mv |
| ZID | Differential input impedance |  | 80 |  | 125 | Ω |
| **LP Line Receiver DC Specifications** | | | | | | |
| VIL | Input low voltage |  |  |  | 550 | mv |
| VIh | Input high voltage |  | 880 |  |  | mv |
| VHYST | Input hysteresis |  | 25 |  |  | mv |
| **Contention Line Receiver DC Specifications** | | | | | | |
| VILF | Input low fault threshold |  |  |  | 200 | mv |
| VIHF | Input high fault threshold |  | 450 |  |  | mv |
| **HS Line Drivers AC Specifications** | | | | | | |
| FDDRCLK | DDR CLK frequency | On CLKP/N outputs | 40 |  | 750 | MHz |
| UIINST | UI instantaneous | Note3 |  |  | 12.5 | ns |
| ΔUI | UI variation | Note4 | -10% |  | 10% | UI |
| Note5 | -5% |  | 5% | UI |
| tCDC | DDR CLK duty cycle | tCDC=tCPH/PDDRCLK |  | 50 |  | % |
| tCPH | DDR CLK high time |  |  | 1 |  | UI |
| tCPL | DDR CLK low time |  |  | 1 |  | UI |
| - | DDR CLK / DATA Jitter | Note6 |  | 75 |  | ps pk-pk |
| tSKEW[PN] | Intra-Pair (Pulse) skew |  |  | 0.075 |  | UI |
| tSKEW[TX] | Data to Clock Skew | Note7 | -0.15 |  | 0.15 | UI |
| Note8 | -0.20 |  | 0.20 | UI |
| tSETUP[RX] | Data to Clock Receiver Setup time | Note9 | 0.15 |  |  | UI |
| Note10 | 0.20 |  |  | UI |
| tHOLD[RX] | Clock to Data Receiver Hold time | Note9 | 0.15 |  |  | UI |
| Note10 | 0.20 |  |  | UI |
| tr | Differential output signal rise time | 20% to 80%, RL = 50Ω, Note11 |  |  | 0.30 | UI |
| 20% to 80%, RL = 50Ω, Note12 |  |  | 0.35 | UI |
| 20% to 80%, RL = 50Ω, Note13 | 100 |  |  | ps |
| tf | Differential output signal fall time | 20% to 80%, RL = 50Ω, Note11 |  |  | 0.30 | UI |
| 20% to 80%, RL = 50Ω, Note12 |  |  | 0.35 | UI |
| 20% to 80%, RL = 50Ω, Note13 | 100 |  |  | ps |
| ΔVCMTX(HF) | Common level variation above 450 MHz | 80Ω≤RL≤125Ω |  |  | 15 | mVrms |
| ΔVCMTX(LF) | Common level variation between 50 MHz and 450 MHz | 80Ω≤RL≤125Ω |  |  | 25 | mVp |
| **LP Line Drivers AC Specifications** | | | | | | |
| trlp , tflp | Single ended output rise/fall time | 15% to 85%, CL < 70 pF |  |  | 25 | ns |
| treot |  | 30% to 85%, CL < 70 pF |  |  | 35 | ns |
| ∂V/∂tSR | Signal slew rate | 15% to 85%, CL < 70 pF,Note14 |  |  | 150 | mV/ns |
| CL | Load capacitance | Note15 | 0 |  | 70 | pF |
| **HS Line Receiver AC Specifications** | | | | | | |
| ΔVCMRX(HF) | Common mode interference beyond 450 MHz |  |  |  | 200 | mVpp |
| ΔVCMRX(LF) | Common mode interference between 50 MHz and 450 MHz |  | -50 |  | 50 | mVpp |
| CCM | Common mode termination | Note16 |  |  | 60 | pF |
| **LP Line Receiver AC Specifications** | | | | | | |
| eSPIKE | Input pulse rejection |  |  |  | 300 | V.ps |
| TMIN | Minimum pulse response |  | 20 |  |  | ns |
| VINT | Pk-to-Pk interference voltage |  |  |  | 400 | mVpp |
| fINT | Interference frequency |  | 450 |  |  | MHZ |
| **Note** | 1. VGNDSH(min) ≤ VI ≤ VGNDSH(max) + VOH(absmax) . Lane module in LP receive mode.  2. 80Ω≤RL≤125Ω  3. This value corresponds to a minimum Mbps data rate.  4. When UI ≥ 1ns, within a single burst.  5. When UI < 1ns, within a single burst.  6. Jitter specification with clean clock at REFCLK input.  7. Total silicon and package skew delay budget of 0.3\*UIINST when D-PHY is supporting maximum data rate = 1 Gbps.  8. Total silicon and package skew delay budget of 0.4\* UIINST when D-PHY is supporting maximum data rate > 1 Gbps.  9. Total setup and hold window for receiver of 0.3\* UIINST when D-PHY is supporting maximum data rate = 1 Gbps.  10. Total setup and hold window for receiver of 0.4\* UIINST when D-PHY is supporting maximum data rate > 1 Gbps.  11. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).  12. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).  13. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.  14. Measured as average across any 50 mV of the output signal transition.  15. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.  16. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification. | | | | | |

## DDR Electrical Characteristics

## Absolute Maximum DC Ratings

|  |  |  |  |
| --- | --- | --- | --- |
| Symbol | Description | Rating | Units |
| DDR\_VDD\_AMAX | Voltage on VDD pin relative to VSS | -0.5 to 1.05 | V |
| DDR\_VDDQ\_AMAX | Voltage on VDDQ pin relative to VSS | -0.5 to 1.98 | V |
| DDR\_PLL\_AMAX | Voltage on VAA\_PLL pin relative to VSS | -0.5 to 1.98 | V |

## Recommended Operating Condition

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Symbol | Parameter | Min | Typ | Max | Units |
| DDR\_VDD\_PLL | PLL and SSTL receiver supply voltage | 1.62 | 1.8 | 1.98 | V |
| DDR\_VDDQ\_4 | SSTL output supply voltage (DDR4) | 1.14 | 1.2 | 1.26 | V |
| DDR\_VDDQ\_3 | SSTL output supply voltage (DDR3) | 1.425 | 1.5 | 1.575 | V |
| DDR\_VDDQ\_3L | SSTL output supply voltage (DDR3L) | 1.283 | 1.35 | 1.45 | V |
| DDR\_VDDQ\_3U | SSTL output supply voltage (DDR3U) | 1.19 | 1.25 | 1.31 | V |
| DDR\_VDDQ\_L3 | SSTL output supply voltage (LPDDR3) | 1.14 | 1.2 | 1.3 | V |
| DDR\_VDDQ\_LP | SSTL output supply voltage (LVCMOS) | 1.65 | 1.8 | 1.95 | V |
| DDR\_VREF | SSTL reference supply voltage | 0.49\*VDDQ | 0.5\*VDDQ | 0.51\*VDDQ | V |
| DDR\_VTT | External termination voltage | VREF-40mV | VREF | VREF+40mV | V |
| DDR\_T | Junction temperature | -40 | 25 | 125 | ℃ |

## DC Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Symbol | Parameter | Min | Typ | Max | Units |
| DDR4\_Mode | DDR\_VIH(DC) | DC input voltage High | VREF+0.1 |  | VDDQ | V |
| DDR\_VIL(DC) | DC input voltage Low | VSSQ |  | VREF-0.1 | V |
| DDR\_VOH | DC output logic High | 0.9\*VDDQ |  |  | V |
| DDR\_VOL | DC output logic Low |  |  | 0.1\*VDDQ | V |
| DDR\_RTT | Input termination resistance (ODT) to VDDQ | 200 | 240 | 280 | ohm |
| 100 | 120 | 140 |
| 67 | 80 | 93 |
| 50 | 60 | 70 |
| 42 | 48 | 56 |
| 34 | 40 | 46 |
| 28 | 34 | 40 |
| DDR3\_Mode | DDR\_VIH(DC) | DC input voltage High | VREF+0.1 |  | VDDQ | V |
| DDR\_VIL(DC) | DC input voltage Low | VSSQ-0.3 |  | VREF-0.1 | V |
| DDR\_VOH | DC output logic High | 0.8\*VDDQ |  |  | V |
| DDR\_VOL | DC output logic Low |  |  | 0.2\*VDDQ | V |
| DDR\_RTT | Input termination resistance (ODT) to VDDQ/2 | 100 | 120 | 140 | ohm |
| 54 | 60 | 66 |
| 36 | 40 | 44 |
| DDR3L\_Mode | DDR\_VIH(DC) | DC input voltage High | VREF+0.09 |  | VDDQ | V |
| DDR\_VIL(DC) | DC input voltage Low | VSSQ-0.3 |  | VREF-0.09 | V |
| DDR\_VOH | DC output logic High | 0.8\*VDDQ |  |  | V |
| DDR\_VOL | DC output logic Low |  |  | 0.2\*VDDQ | V |
| DDR\_RTT | Input termination resistance (ODT) to VDDQ/2 | 100 | 120 | 140 | ohm |
| 54 | 60 | 66 |
| 36 | 40 | 44 |
| LPDDR3\_Mode | DDR\_VIH(DC) | DC input voltage High | VREF+0.1 |  | VDDQ | V |
| DDR\_VIL(DC) | DC input voltage Low | VSSQ |  | VREF-0.1 | V |
| DDR\_VOH | DC output logic High | 0.9\*VDDQ |  |  | V |
| DDR\_VOL | DC output logic Low |  |  | 0.1\*VDDQ | V |
| DDR\_RTT | Input termination resistance (ODT) to VDDQ | 100 | 120 | 140 | ohm |
| 200 | 240 | 280 |

## Recommended Operating Frequency

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Symbol | Parameter | Condition | Min | Typ | Max | Unit |
| DDR4\_Mode | ddr\_data\_rate | DDR data rate | 1.0V, 25℃ |  |  |  | Mbps |
| 1.1V, -40℃ |  |  |  |
| 0.9V, 125℃ |  |  | 2400 |
| DDR3\_Mode | ddr\_data\_rate | DDR data rate | 1.0V, 25℃ |  |  |  | Mbps |
| 1.1V, -40℃ |  |  |  |
| 0.9V, 125℃ |  |  | 2133 |
| DDR3L\_Mode | ddr\_data\_rate | DDR data rate | 1.0V, 25℃ |  |  |  | Mbps |
| 1.1V, -40℃ |  |  |  |
| 0.9V, 125℃ |  |  | 1866 |
| LPDDR3\_Mode | ddr\_data\_rate | DDR data rate | 1.0V, 25℃ |  |  |  | Mbps |
| 1.1V, -40℃ |  |  |  |
| 0.9V, 125℃ |  |  | 2133 |

## Electrical Characteristics for DDR IO

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Symbol | Parameter | Min | Typ | Max | Units |
| DDR4\_Mode | DDR\_C\_IO | I/O capacitance (equivalent at VDDQ/2) | 1.94 | 1.97 | 2.11 | pF |
| DDR\_PRCVQ\_AC | Input mode AC power (VDDQ rail) | 0.17 | 0.20 | 0.23 | uW/MHz |
| DDR\_PRCV\_AC | Input mode AC power (VDD rail) | 0.13 | 0.15 | 0.22 | uW/MHz |
| DDR\_PDRVQ\_AC | Output mode AC power (VDDQ rail) | 8.08 | 8.08 | 9.77 | uW/MHz |
| DDR\_PDRV\_AC | Output mode AC power (VDD rail) | 1.34 | 1.67 | 2.27 | uW/MHz |
| DDR3\_Mode | DDR\_C\_IO | I/O capacitance (equivalent at VDDQ/2) | 1.91 | 1.94 | 2.07 | pF |
| DDR\_PRCVQ\_AC | Input mode AC power (VDDQ rail) | 0.20 | 0.21 | 0.24 | uW/MHz |
| DDR\_PRCV\_AC | Input mode AC power (VDD rail) | 0.13 | 0.15 | 0.19 | uW/MHz |
| DDR\_PDRVQ\_AC | Output mode AC power (VDDQ rail) | 10.83 | 10.83 | 12.35 | uW/MHz |
| DDR\_PDRV\_AC | Output mode AC power (VDD rail) | 1.35 | 1.68 | 2.27 | uW/MHz |
| DDR3L\_Mode | DDR\_C\_IO | I/O capacitance (equivalent at VDDQ/2) | 1.92 | 1.96 | 2.09 | pF |
| DDR\_PRCVQ\_AC | Input mode AC power (VDDQ rail) | 0.20 | 0.22 | 0.26 | uW/MHz |
| DDR\_PRCV\_AC | Input mode AC power (VDD rail) | 0.13 | 0.15 | 0.22 | uW/MHz |
| DDR\_PDRVQ\_AC | Output mode AC power (VDDQ rail) | 8.43 | 8.43 | 10.76 | uW/MHz |
| DDR\_PDRV\_AC | Output mode AC power (VDD rail) | 1.34 | 1.67 | 2.27 | uW/MHz |
| LPDDR3\_Mode | DDR\_C\_IO | I/O capacitance (equivalent at VDDQ/2) | 1.94 | 1.97 | 2.11 | pF |
| DDR\_PRCVQ\_AC | Input mode AC power (VDDQ rail) | 0.20 | 0.23 | 0.26 | uW/MHz |
| DDR\_PRCV\_AC | Input mode AC power (VDD rail) | 0.12 | 0.15 | 0.22 | uW/MHz |
| DDR\_PDRVQ\_AC | Output mode AC power (VDDQ rail) | 7.38 | 7.38 | 9.17 | uW/MHz |
| DDR\_PDRV\_AC | Output mode AC power (VDD rail) | 1.34 | 1.67 | 2.27 | uW/MHz |

## 

## ABB/PLL Electrical Characteristics

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Reference Clock  Electrical Parameters | Min. | Typ. | Max. | Units | Description |
| External Clock Frequency |  | 20/40 |  | MHz | CLKREF\_SEL\_PAD='0': 40MHz input CLKREF\_SEL\_PAD='1': 20MHz input A 20MHz crystal may also be used |
| Input Duty Cycle | 49 | 50 | 51 | % |  |
| Single-ended clock  input voltage  (CMOS or sinewave) | 0.8 | 1 | 1.2 | V |  |
| frequency accuracy | -20 | 0 | 20 | ppm |  |
| Input Jitter |  |  | 2.5 | ps |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Analog Signal   Electrical Parameters | Min. | Typ. | Max. | Units | Description |
| DAC OUTPUTS | 0 | 0.9 | 1.8 | V | DAC outputs typical 0.65~1.15V |
| ADC INPUTS | 0 | 0.9 | 1.8 | V | ADC inputs typical 0.65~1.15V |
| AD INPUTS | 0 | 0.9 | 1.8 | V | AD inputs typical 0~1.8V |
| Other analog PAD | 0 |  | 1.8 | V |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Analog and PLL  power suppy  Electrical Parameters | Min. | Typ. | Max. | Units | Description |
| AVDD |  | 1.8 | 1.98 | V | 1.8V analog power supply for ABB and PLL |
| AVSS | -0.2 | 0 | 0.2 | V | analog ground for ABB and PLL |